1. Convert 7090.441_{10} to hexadecimal. Carry out your answer to three places past the decimal point.
   7090.441= 1BB2

$(\ 7090\ )_{10} = (\ 1BB2\ )_{16}$
Explanation
Step 1:
Continually divide decimal number by 16 to give a result and a remainder. Write down the remainder (in hexadecimal).

Division	Result	remainder (in dec)	remainder (in hex)
7090 / 16	443	2	**2**
443 / 16	27	11	**B**
27 / 16	1	11	**B**
1 / 16	0	1	**1**

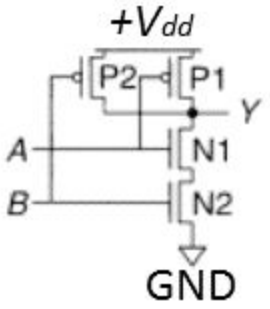
2. Design a minimum two-level NOR-NOR circuit to realize $f(W, X, Y, Z) = \sum m(10, 12, 14)$. Enter the Boolean equation that describes the circuit and attach a Word, PDF, or image file of your circuit in Part 2 of the final exam. Then convert the circuit to two-level NAND-AND circuit. Do not use gate symbols with bubbles in your final answer. Enter the Boolean equation that describes the circuit and attach a Word, PDF, or image file of your circuit in Part 2 of the final exam. Also attach any Karnaugh maps used to derive the equations for the circuit.

3. Find a minimum two-level, NAND gate circuit to simultaneously realize $f_1 = \sum m(3, 4, 6, 8, 11, 12, 15)$ and $f_2 = \sum m(3, 4, 6, 8, 11, 13, 14)$. *Hint*: the minimum solution has nine gates. Enter the equations for f_1 and f_2 and attach files of any Karnaugh maps or other work used to derive the equations. In Part 2 of the final exam, attach a Word, PDF, or image file of your circuit.

f_1 =

f_2 =

4. Complete the truth table for the CMOS logic circuit shown where P_1 and $P_2$are *p*-channel MOSFETS and N_1 and N_2 are *n*-channel MOSFETs. Use 0 or 1 for *Y* and use ON or OFF for P_1, P_2, N_1, and N_2. Assume a voltage of V_{dd}applied to *Y* produces an output of 1. State what type of device this is (i.e., Inverter, NAND Gate, or NOR Gate).



A	*B*	*P1*	*P2*	*N1*	*N2*	*Y*
0	0					
0	1					
1	0					
1	1					

5. Write the logic equation for the output described by the truth table below for an 8-to-1 MUX with control inputs *A, B,* and *C*.

A	*B*	*C*	*Y*
0	0	0	1
0	0	1	1

0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

6. What is the difference between a D latch and a D flip-flop?

(a) There is no difference between a latch and a flip-flop. They both accomplish the same purpose with different circuits.

(b) A latch allows input to flow through *D* to the output *Q* at the clock edge and a flip-flop allows input *D* to flow through to the output *Q* when the clock is high.

(c) A latch allows input to flow through *D* to the output *Q* when the clock is high and a flip-flop allows input *D* to flow through to the output *Q* at the clock edge.

(d) A latch “latches” the output to the intended value and a flip-flop “flip-flops” the output to the opposite value

7. What is a D-CE flip-flop?

(a) A D flip-flop with a clear function.

(b) A D flip-flop with two additional inputs.

(c) A D flip-flop that uses a clock enable rather than gating the clock.

(d) A D flip-flop with control inputs.

8. Design a 3-bit counter that counts in the sequence: *ABC* = 010, 011, 111, 001, 100, 110, 000, 010, …

Use D flip-flops. Enter your final equations for D_A, D_B, and D_C in the spaces provided and attach any transition tables and next-state maps used to derive them in Part 2 of the final exam.

D_A =

D_B =

D_C =

9. An M-N flip-flop behaves as follows:

If *MN* = 00, the next state of the flip-flop is 0.

If *MN* = 10, the next state of the flip-flop is the same as the present state.

If *MN* = 01, the next state of the flip-flop is the complement of the present state.

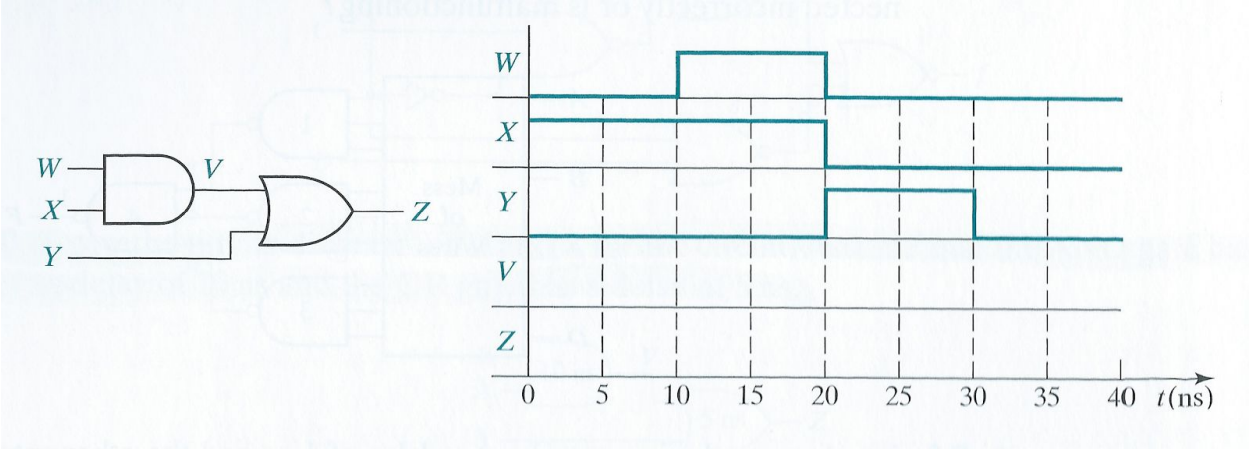
If *MN* = 11, the next state of the flip-flop is 1.

Complete the following table for *M* and *N* using don't-cares when possible.

Present State	**Next State**			
Q	***Q+***	***M***	***N***	***MN***
0	**0**			
0	**1**			

1	**0**			
1	**1**			

10. Complete the timing diagram for the given circuit. The AND gate has a propagation delay of 5 ns, the OR gate has a propagation delay of 12.5 ns, and *V* and *Z* are initially zero. In Part 2 of the final exam, attach a Word, PDF, or image file of your completed diagram.



11. Write a short sentence describing the operation of the state machine shown in the figure below.